

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kie Y. Ahn et al.
Title: MULTILEVEL COPPER INTERCONNECT WITH DOUBLE PASSIVATION

Docket No.: 303.685US2 Serial No.: 10/721920
Filed: November 24, 2003 Due Date: N/A
Examiner: Michael Trinh Group Art Unit: 2822

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

·We are transmitting herewith the following attached items (as indicated with an "X"):

A return postcard.
 A Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (4 pgs.), and copies of 51 cited documents.

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Customer Number 21186

By: Suneel Arora
Atty: Suneel Arora
Reg. No. 42,267

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(GENERAL)



PATENT

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
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In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Supplemental Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Supplemental Information Disclosure Statement considered.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

The present application is either a U.S. national patent application filed after June 30, 2003 or an international application that entered the national stage under 35 U.S.C. § 371 after June 30, 2003. Thus, Applicant believes that the U.S. Patent & Trademark Office has waived the requirement under 37 C.F.R. 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication. The waiver is provided in a pre-OG notice from the U.S. Patent & Trademark Office entitled "Information Disclosure Statements May Be Filed Without Copies of U.S. Patents and Published Applications in Patent Applications filed after June 30, 2003" and dated July 11, 2003. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

Respectfully submitted,

KIE Y. AHN ET AL.

By their Representatives,

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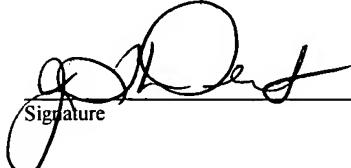
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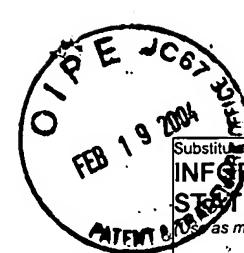
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Group Art Unit	2822
Examiner Name	Trinh, Michael

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Attorney Docket No: 303.685US2

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

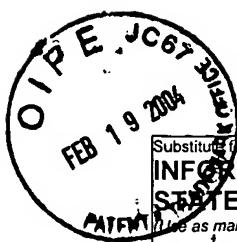
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Substitute Disclosure Statement Form (PTO-1449)

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached



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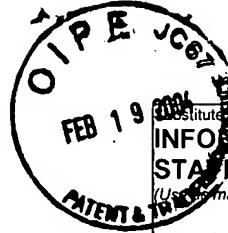
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